

DC-DC Converter, Non-Isolated**DAM60N12D0V6GSGA****5Vdc to 14Vdc Input; 0.6 ~2.0Vdc/ 60 A Output****RoHS Compliant****Applications**

- Wireless Networks
- Access and Optical Network Equipment
- Enterprise Networks
- Latest generation IC's (DSP, FPGA, ASIC) and Microprocessor powered applications

Feature

- Compliance with RoHS10 EU Directive 2011/65/EU & (EU)2015/863
- Delivers up to 60A output current
- High efficiency: typ. 88.5% at 12Vin, 1.0Vout
- Small size and profile 1.38x0.62x0.35 (inch)
- Low output ripple and noise
- Exceptional thermal performance
- Power good signal
- Lead free HASL
- Switching frequency 400kHz
- Output voltage programmable from 0.6Vdc to 2.0Vdc via external resistor.
- High reliability
- Remote On/Off
- Input under voltage protection
- Output over current protection
- Short circuit protection
- Over temperature protection
- Meets IEC/UL/EN60950-1

Description

DAM60N12D0V6GSGA is a non-isolated DC/DC converter that provides a high efficiency single output. It can operate from 5Vdc to 14Vdc input and 0.6Vdc~2.0Vdc/60A output. Features include remote On/Off, adjustable output voltage, over current and overtemperature protection.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Units	Specifications			Notes & conditions
		Min.	Typ.	Max.	
Input Voltage	Vdc	-0.3	-	15	Continuous
Operating Ambient Temperature	°C	-40	-	85	Forced air cooling
Storage Temperature	°C	-55	-	125	
Operating Humidity	RH(%)	10	-	90	Non-condensing
Storage Humidity	RH(%)	10	-	90	Non-condensing
Operating Altitude	m	0	-	3000	
Storage Altitude	m	0	-	3000	

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and room temperature conditions.

Input Characteristics

Parameter	Units	Specifications			Notes & conditions
		Min.	Typ.	Max.	
Operating Input Voltage	Vdc	5	12	14	
Maximum Input Current	A	-	-	30	Vin=5V to 14V, Io=Io(max)
Input No load Current	mA	-	100	-	Vin=Vin(nom), Io=0, module enabled Vo=0.6V
	mA	-	180	-	Vin=Vin(nom), Io=0, module enabled Vo=2V
Input Stand-by Current	mA	-	12.5	-	Vin=Vin(nom), module enabled
Input Reflected Ripple Current (Peak-to-Peak)	mA	-	250	-	5Hz to 20MHz bandwidth, 1uH source impedance, Vin=5V to 14V. Io=Io(max)

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Inrush Transient	A ² S	-	-	1	
Input fuse	A	-	-	30	

Remote Control Characteristics

Parameter		Units	Specifications			Notes & conditions
			Min.	Typ.	Max.	
Positive Logic	Logic High Voltage	Vdc	3.5	-	VinMax	
	Logic Low Voltage	Vdc	-0.3	-	0.4	
Negative Logic	Logic High Voltage	Vdc	2	-	VinMax	
	Logic Low Voltage	Vdc	-0.2	-	0.4	

Output Characteristics

Parameter		Units	Specifications			Notes & conditions
			Min.	Typ.	Max.	
Output Voltage set point		%Vo	-	-	±1	With 0.1% tolerance for external resistor used to set output voltage
Output Current		A	0	-	60	
Line Regulation		mV	-	6	-	Vin=Vin(min) to Vin(max)
Load Regulation		mV	-	10	-	Io=Io(min) to Io(max)
Output Voltage Range		%Vo	-	±2	-	Over all operating input voltage, resistive load, and temperature conditions until end of life
Output Adjustment Range		Vdc	0.6	-	2.0	
Output Current Limit		%Io	-	130	-	
Temperature Coefficient		%/°C	-	0.4	-	-40°C~85°C
External Capacitive Load	Without the Tunable Loop	µF	4x47	-	6x47	ESR≤1mΩ

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Ripple and Noise	mVp-p	-	50	70	Vin=Vin(nom), Io=Io(min) to Io(max), measured with 0.1 μ F ceramic and 47 μ F ceramic capacitors in parallel 20MHz bandwidth
	mVrms	-	15	-	
Dynamic Response	mV/ μ S	-	300/60	-	25%~75%~25%load step, di/dt=2.5A/ μ s
Turn-on Delay Time	ms	-	6	-	Delay from instant at which Vin=Vin(min) until Vo=10% of Vo(nom)
Turn-on Rise Time	ms	-	1	-	Time for Vo to rise from 10% of Vo(nom) to 90% of Vo(nom)

Protection Characteristics

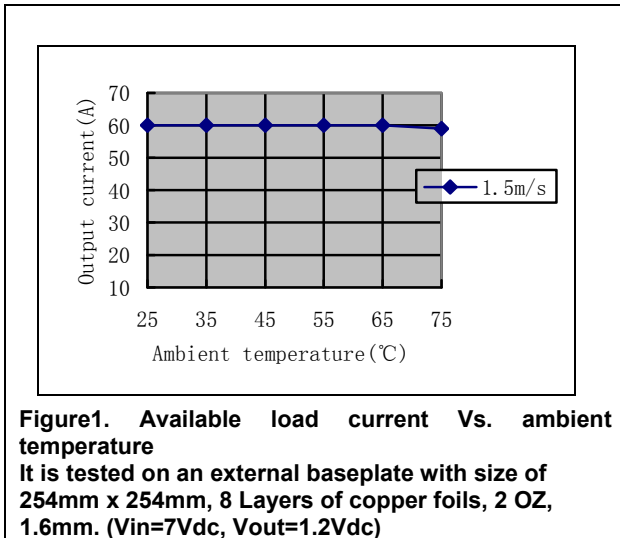
Parameter		Units	Specifications			Notes & conditions
			Min.	Typ.	Max.	
Input Undervoltage Lockout	Turn-on Threshold	Vdc	-	5	-	
	Turn-off Threshold	Vdc	-	4.5	-	
	Hysteresis	Vdc	-	0.5	-	
Output Over Current Protection		-	-	Yes	-	Hiccup mode
Short Circuit Protection		-	-	Yes	-	Hiccup mode Automatic recovery
Over Temperature Protection		$^{\circ}$ C	-	125	-	See Thermal Consideration section
Over Temperature Protection Hysteresis		$^{\circ}$ C	-	5	-	
Pulldown Resistance of PGOOD Pin		Ω	-	-	50	
Sink Current Capability Into PGOOD Pin		mA	-	-	5	
PG_DELAY Time	PGood ON	us	-	50	-	

General Specifications

Parameter		Units	Specifications			Notes & conditions
			Min.	Typ.	Max.	
Efficiency	Vo=0.6V	%	78.0	81.3	-	Vin=12Vdc, Io=Io(max) 25°C, Vo=Vo(nom)
	Vo=1.0V	%	86	88.5	-	
	Vo=1.8V	%	85.25	91.5	-	
Switching Frequency		kHz	380	400	420	
MTBF		Hour	6,498,438			Io=0.8Io(max), 40°C Telecordia Issue 2 Method 1 Case 3
Thermal Stability Time		min	-	30	-	
Weight		g	-	18	-	
Safety		Compliant to IEC60950-1,UL60950-1,EN60950-1 and GB4943				
Vibration		IEC60068-2-6:10-500Hz sweep,0.75mm excursion,10g acceleration,10minutes in each 3 perpendicular directions				
Transportation		ETS300019-1-2				
Shock		IEC60068-2-27:200g acceleration, duration 3 ms,6 drops in each 3 perpendicular directions				

Characteristic Curves

Derating



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Test Configurations

Input Filtering

The module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 2 shows the input ripple voltage for various output voltages at 60A of load current with 4x22 μ F, 6x22 μ F or 8x22 μ F ceramic capacitors and an input of 12V.

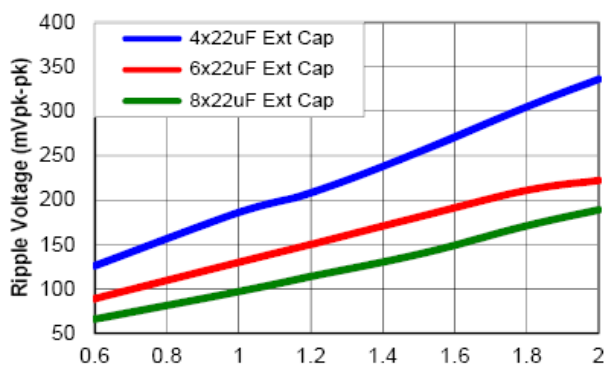


Figure2. Input ripple voltage for various output voltages with various external ceramic capacitors at the input (60A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz

Output Filtering

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1 μ F ceramic and 47 μ F ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons.

First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 3 provides output ripple information for different external capacitance values at various V_o and a full load current of 60A. For stable

operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table.

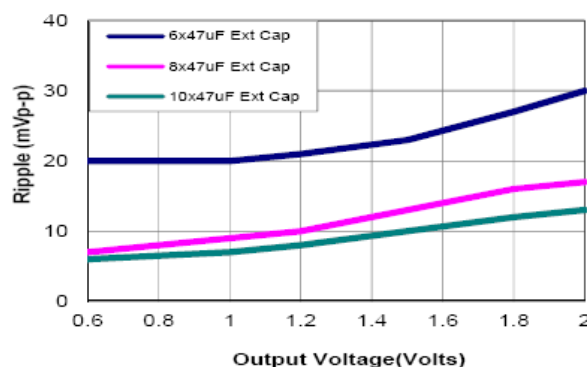


Figure3. Output ripple voltage for various output voltages with external 6x47 μ F, 8x47 μ F or 10x47 μ F ceramic capacitors at the output (60A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1, CSA C22.2 No. 60950-1-03, and VDE 0850:2001-12 (EN60950-1) Licensed.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV. The input to these units is to be provided with a fast-acting fuse with a maximum rating of 30A in the positive input lead.

Feature Descriptions

Remote On/Off

Two On/Off logic options are available. In the Positive Logic On/Off option, the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using

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the On/Off pin is shown in Figure 4.

For negative logic On/Off modules, the circuit configuration is shown in Fig. 5.

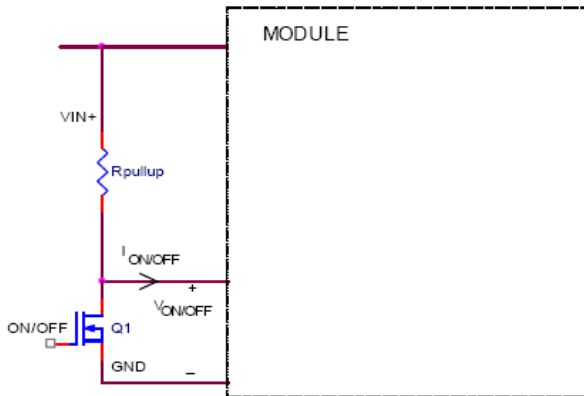


Figure 4. Circuit configuration for using positive On/Off logic.

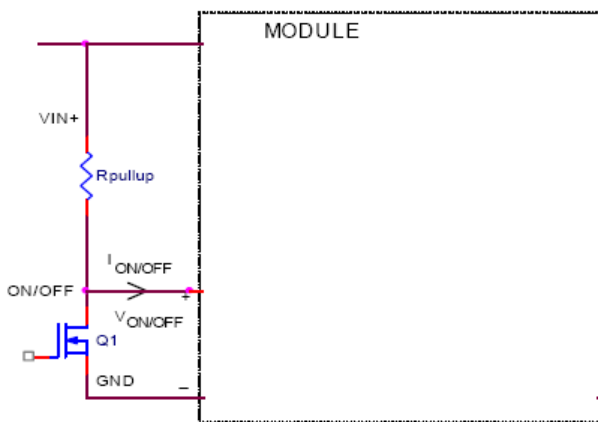


Figure 5. Circuit configuration for using negative On/Off logic.

Monotonic Start-up and Shutdown

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

Startup into Pre-biased Output

The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

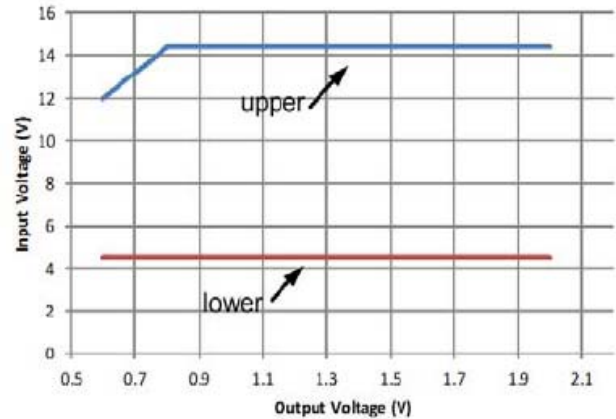


Figure 6. Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

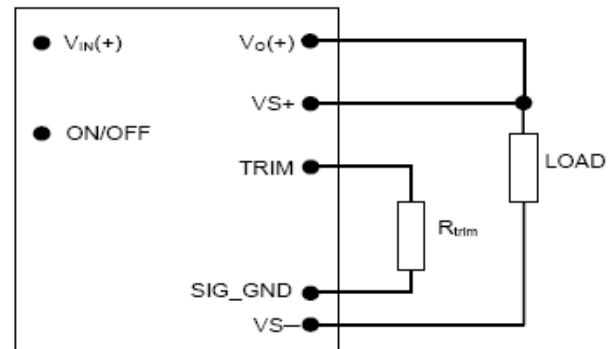


Figure 7. Circuit configuration for programming output voltage using an external resistor.

Without an external resistor between Trim and SIG_GND pins, the output of the module will be 0.6Vdc. To calculate the value of the trim resistor, R_{trim} for a desired output voltage, should be as per the following equation:

$$R_{trim} = \left[\frac{0.6}{(V_o - 0.6)} \right] K\Omega$$

R_{trim} is the external resistor in $k\Omega$

V_o is the desired output voltage.

Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the VOUT and GND pins of the module should not exceed 0.5V.

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Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, $R_{margin-up}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{margin-down}$, from the Trim pin to output pin for margining-down. Figure 8 shows the circuit configuration for output voltage margining.

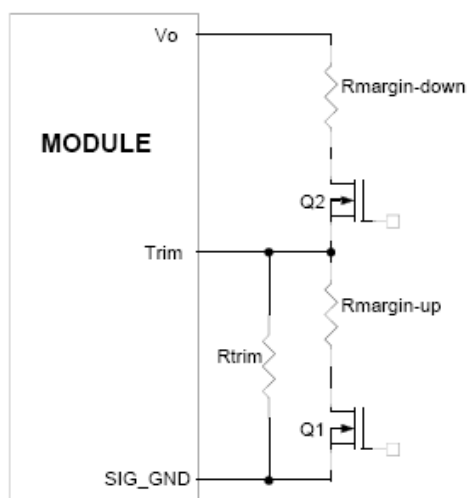


Figure 8. Circuit Configuration for margining Output voltage.

PMBus Addressing

To properly set the device addresses, resistors with 1% tolerance must be connected from the ADDR0 and ADDR1 pins to ground. Once a valid PMBus address has been determined, communication with the controller can be established via the PMBus bus of the controller.

Table 1: Device PMBus Address

Resistor-to-GND(1%)	ADDR1								
	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open	
ADDR0	2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
	2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
	3.16 kΩ	F4	D4	B4	94	74	54	34	14
	4.02 kΩ	F0	D0	B0	90	70	50	30	10
	5.36 Ω	EC	CC	AC	8C	6C	4C	2C	0C
	8.06 Ω	E8	C8	A8	88	68	48	28	08
	16.0 kΩ	E4	C4	A4	84	64	44	24	04
	Open	E0	C0	A0	80	60	40	20	reserved

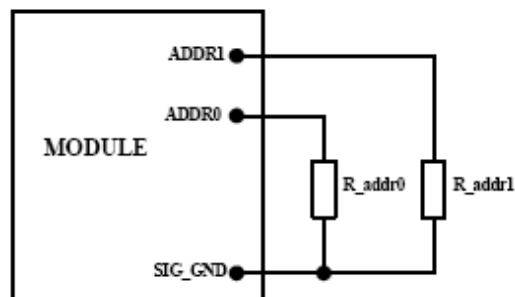


Figure 9. Circuit showing connection of resistors used to set the PMBus address of the module.

Protection Features

Input Under Voltage Protection

At input voltages below the input under-voltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the under-voltage lockout turn-on threshold.

Output Over Current Protection

To provide protection in an output overload fault condition, the module is equipped with internal current-limiting circuitry and can endure current limiting for an unlimited duration. At the instance of current-limit inception, the module enters a "hiccup" mode of operation, whereby it shuts down and automatically attempts to restart. While the fault condition exists, the module will remain in this mode until the fault is cleared. The unit operates normally once the output current is reduced back into its specified range.

Over Temperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of OTP set value is exceeded at the thermal reference point T_{ref} . Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as over-temperature, overcurrent or loss of regulation occurs that would result in the output

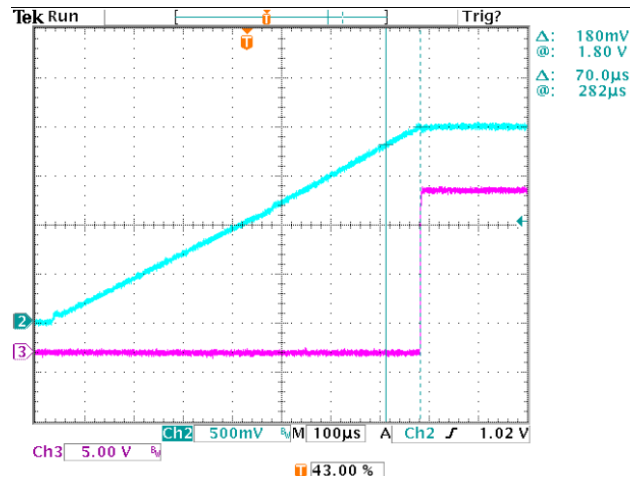
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voltage going outside the specified thresholds.

The default value of PGOOD ON thresholds are set at $\pm 8\%$ of the nominal Vset value, and PGOOD OFF thresholds are set at $\pm 10\%$ of the nominal Vset. For example, if the nominal voltage (Vset) is set at 1.0V, then the PGOOD ON thresholds will be active anytime the output voltage is between 0.92V and 1.08V, and PGOOD OFF thresholds are active at 0.90V and 1.10V respectively.

The PGOOD terminal can be connected through a pull-up resistor (suggested value 100K) to a source of 5VDC or lower.



Summary of Supported PMBus Commands

Hex Code	Command	Brief Description	Non-Volatile Memory Storage																																													
01	OPERATION	<p>Turns Module on or off in conjunction with the input from the CONTROL (VR_ENABLE) pin.</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Unsigned Binary</th> </tr> <tr> <th>Bit Position</th> <th>7</th> <th>6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Access</td> <td>r/w</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>On</td> <td>X</td> <td colspan="4">Margin</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r	r/w	r/w	r/w	r/w	r	r	Function	On	X	Margin				X	X	Default Value	1	0	0	0	0	0	0	0	
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Default Value	1	0	0	0	0	0	0	0																																								
02	ON_OFF_CONFIG	<p>Configures the ON/OFF functionality as a combination of analog ON/OFF pin and.</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Unsigned Binary</th> </tr> <tr> <th>Bit Position</th> <th>7</th> <th>6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> </tr> <tr> <td>Function</td> <td>X</td> <td>X</td> <td>X</td> <td>pu</td> <td>cmd</td> <td>cpr</td> <td>pol</td> <td>cpa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r/w	r/w	r/w	r/w	r	Function	X	X	X	pu	cmd	cpr	pol	cpa	Default Value	0	0	0	1	0	1	1	0	YES
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Default Value	0	0	0	1	0	1	1	0																																								
03	CLEAR_FAULTS	Clears any fault bits that may have been set, also releases the SMBALERT# signal if the device has been asserting it.																																														
10	WRITE_PROTECT	<p>Used to control writing to the module via PMBus. Copies the current register setting in the module whose command code matches the value in the data byte into nonvolatile.</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Unsigned Binary</th> </tr> <tr> <th>Bit Position</th> <th>7</th> <th>6</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Function</td> <td>bit7</td> <td>bit6</td> <td>bit5</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> </tbody> </table> <p>Bit5: 0 – Enables all writes as permitted in bit6 or bit7 1 – Disables all writes except the WRITE_PROTECT, OPERATION Bit6 0– Enables all writes as permitted in bit5 or bit7 1 – Disables all writes except for the WRITE_PROTECT and PERATION commands (bit5 and bit7 must be 0) Bit7: 0 – Enables all writes as permitted in bit5 or bit6 1 – Disables all writes except for the WRITE_PROTECT command(bit5 and bit6 must be 0)</p>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	X	X	X	X	X	Function	bit7	bit6	bit5	X	X	X	X	X	Default Value	0	0	0	X	X	X	X	X	YES
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Default Value	0	0	0	X	X	X	X	X																																								
15	STORE_USER_ALL	To start a Global Upload. During download, all PMBus writes/reads are NACKed.																																														
16	RESTORE_USER_ALL	To start a Global Download. During download, all PMBus writes/reads are NACKed.																																														

20	VOUT_MODE	<p>The module has MODE set to Linear and Exponent set to -10. These values cannot be changed.</p> <table border="1" data-bbox="475 472 1145 667"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Mode</td> <td colspan="4">Exponent</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mode				Exponent				Default Value	0	0	1	0	0	0	0	1																																					
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21	VOUT_COMMAND	<p>Sets the output Voltage of the unit, when OPERATION is set to “ON, without margining”. VID format. VOUT_COMMAND register is shared between SVID and PMBus VID sources.</p> <table border="1" data-bbox="475 770 1219 1128"> <tr> <td>Format</td> <td colspan="8">VID format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	VID format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	0	0	0	0	0	YES
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Function	Low Byte																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
24	VOUT_MAX	<p>Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. VID format.</p> <table border="1" data-bbox="475 1227 1145 1585"> <tr> <td>Format</td> <td colspan="8">VID format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	Format	VID format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	1	1	1	1	1	1	1	1	YES
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Default Value	1	1	1	1	1	1	1	1																																																																												

25	VOUT_MARGIN_HI GH	<p>Sets the target voltage for margining the output high.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">VID format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	VID format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	0	0	0	0	0	YES
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26	VOUT_MARGIN_L OW	<p>Sets the target voltage for margining the output low.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">VID format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	VID format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	0	0	0	0	0	YES
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27	VOUT_TRANSITIO N_RATE	<p>Sets the rate in mV/μs(Literal Format) at which the output should change voltage.(Range:0 ~ 50)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	1	0	1	0	YES
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Default Value	0	0	0	0	1	0	1	0																																																																												

28	VOUT_DROOP	<p>Sets the rate at which the output voltage decreases, in mW (Literal Format) with increasing current. (Range:0 ~19.99)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Exponent				Mantissa				Default Value	1	0	0	1	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	YES
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Default Value	0	0	0	0	0	0	0	0																																																																												
32	MAX_DUTY	<p>Sets the maximum duty cycle, in % (Literal Format), of the unit's power conversion stage. (Range:0 ~99.61)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	1	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	1	0	0	1	0	0	0	0	YES
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Default Value	1	0	0	1	0	0	0	0																																																																												
35	VIN_ON	<p>Sets the value of input voltage at which the module turns on. (Range:0 ~31.875)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	1	0	1	0	0	0	YES
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Function	Mantissa																																																																																			
Default Value	0	0	1	0	1	0	0	0																																																																												

36	VIN_OFF	<p>Sets the value of input voltage at which the module turns off. (Range:0 ~31.875)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	1	0	0	1	0	0	YES
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Function	Mantissa																																																																																			
Default Value	0	0	1	0	0	1	0	0																																																																												
40	VOUT_OV_FAULT_LIMIT	<p>Sets the value of the average sensed output voltage, in V (Literal Format) that causes a "fixed" over-voltage fault. Exponent is fixed at -10.Suggested value shown for 1.2Vo. Should be changed for different output voltage. (Range:0 ~3.05) Values can be 108%, 110%, 112% or 115% of output voltage.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	High Byte								Default Value	1	1	0	0	0	1	0	1	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	0	0	1	0	1	1	0	YES
Format	Literal Format. two's complement binary																																																																																			
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41	VOUT_OV_FAULT_RESPONSE	<p>Sets the response type to an output over-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td><td>RS P [0]</td><td>RS [2]</td><td>RS [1]</td><td>RS [0]</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	1	0	1	1	1	0	0	1	YES																																				
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Default Value	1	0	1	1	1	0	0	1																																																																												
44	VOUT_UV_FAULT_LIMIT	<p>Sets the value of the average sensed output voltage, in V (Literal Format) that causes Vout under-voltage fault. Exponent is fixed at -10.Suggested value shown for 1.2Vo. Should be changed for different output voltage.(Range:0 ~3.05) Values can be 92%, 90%, 88% or 85% of output voltage</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	YES																																																															
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		<table border="1"> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	High Byte								Default Value	1	1	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Low Byte								Default Value	0	1	0	0	0	0	0	0																			
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45	VOUT_UV_FAULT_RESPONSE	<p>Sets the response type to an output under-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td> <td>RS P [0]</td> <td>RS [2]</td> <td>RS [1]</td> <td>RS [0]</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	1	0	1	1	1	0	0	1	YES																																				
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Default Value	1	0	1	1	1	0	0	1																																																																												
46	IOUT_OC_FAULT_LIMIT	<p>Sets the value of the averaged sensed total output current in PS0 power state, in A (Literal Format), that causes an over-current fault. (Range:0 ~1023)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	1	0	1	1	1	1	1	YES
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47	IOUT_OC_FAULT_RESPONSE	<p>Sets the response type to an output over-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td> <td>RS P [0]</td> <td>RS [2]</td> <td>RS [1]</td> <td>RS [0]</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	0	0	1	1	1	0	0	1	YES																																				
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Default Value	0	0	1	1	1	0	0	1																																																																												

4F	OT_FAULT_LIMIT	<p>Sets the value of the external sense temperature, in °C (Literal Format) that causes an over-temperature fault. (Range:0 ~255)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	1	1	1	1	1	0	1	YES
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50	OT_FAULT_RESPONSE	<p>Sets the response type to an output over-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td> <td>RS P [0]</td> <td>RS [2]</td> <td>RS [1]</td> <td>RS [0]</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	1	0	0	0	0	0	0	0	YES																																				
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Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X																																																																												
Default Value	1	0	0	0	0	0	0	0																																																																												
51	OT_WARN_LIMIT	<p>Sets the value of the external sense temperature, in °C (Literal Format) that causes an over-temperature warning. (Range:0 ~255)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	1	1	0	1	1	1	0	YES
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Function	Mantissa																																																																																			
Default Value	0	1	1	0	1	1	1	0																																																																												

55	VIN_OV_FAULT_LI MIT	<p>Sets the value of the measured input voltage, in V (Literal Format) that causes an input over-voltage fault. (Range:0 ~31.875)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	1	1	1	1	0	0	0	YES
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Default Value	0	1	1	1	1	0	0	0																																																																												
56	VIN_OV_FAULT_RE SPONSE	<p>Sets the response type to an input over-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td> <td>RS P [0]</td> <td>RS [2]</td> <td>RS [1]</td> <td>RS [0]</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	1	0	0	0	0	0	0	0	YES																																				
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Default Value	1	0	0	0	0	0	0	0																																																																												
59	VIN_UV_FAULT_LI MIT	<p>Sets the value of the measured input voltage, in V (Literal Format) that causes an input over-voltage fault. (Range:0 ~31.875)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	1	0	0	1	0	0	YES
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5A	VIN_UV_FAULT_RE SPONSE	<p>Sets the response type to an input under-voltage fault.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r/w</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td>RS P [1]</td> <td>RS P [0]</td> <td>RS [2]</td> <td>RS [1]</td> <td>RS [0]</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r/w	r/w	r/w	r/w	r/w	r	r	r	Function	RS P [1]	RS P [0]	RS [2]	RS [1]	RS [0]	X	X	X	Default Value	1	0	0	0	0	0	0	0	YES																																				
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Default Value	1	0	0	0	0	0	0	0																																																																												

60	TON_DELAY	<p>Sets the time, in ms (Literal Format), from when a start condition is received until the output voltage starts to rise. (Range:0 ~51)</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	Function	Mantissa								Default Value	0	0	0	0	0	0	1	1	YES
Format	Literal Format. two's complement binary																																																																																			
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Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	1	1																																																																												
78	STATUS_BYTE	<p>Returns one byte of information with a summary of the most critical faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Flag</td> <td>x</td><td>OF F</td><td>OO VP</td><td>OC P</td><td>IUV P</td><td>TE MP</td><td>CM L</td><td>OTHE R</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	x	OF F	OO VP	OC P	IUV P	TE MP	CM L	OTHE R	Default Value	0	0	0	0	0	0	1	1																																					
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Default Value	0	0	0	0	0	0	1	1																																																																												
79	STATUS_WORD	<p>Returns two bytes of information with a summary of the units fault condition.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Flag</td> <td>x</td><td>OF F</td><td>OO VP</td><td>OC P</td><td>IUV P</td><td>TE MP</td><td>CM L</td><td>OTHE R</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function									Default Value	0	0	0	1	0	0	1	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	x	OF F	OO VP	OC P	IUV P	TE MP	CM L	OTHE R	Default Value	0	0	0	0	0	0	1	1	
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Default Value	0	0	0	0	0	0	1	1																																																																												
7A	STATUS_VOUT	<p>Returns one byte of information with the status of the module's output voltage related faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Flag</td> <td>VOUT _OV</td><td>X</td><td>X</td><td>VOU T_UV</td><td>VOUT_ MAX WARN</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	VOUT _OV	X	X	VOU T_UV	VOUT_ MAX WARN	X	X	X	Default Value	0	0	0	0	0	0	0	0																																					
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Default Value	0	0	0	0	0	0	0	0																																																																												

7B	STATUS_IOUT	<p>Returns one byte of information with the status of the module's output current related faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Flag</td> <td>IOUT_OC</td> <td>X</td> <td>X</td> <td>IOUT_OCW</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	IOUT_OC	X	X	IOUT_OCW	X	X	X	X	Default Value	0	0	0	0	0	0	0	0	
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Flag	IOUT_OC	X	X	IOUT_OCW	X	X	X	X																																								
Default Value	0	0	0	0	0	0	0	0																																								
7C	STATUS_INPUT	<p>Returns one byte of information with the status of the module's input current related faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Flag</td> <td>IOVP</td> <td>X</td> <td>X</td> <td>IUVP</td> <td>OFF</td> <td>IIN_OCP</td> <td>IIN_OCW</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	IOVP	X	X	IUVP	OFF	IIN_OCP	IIN_OCW	X	Default Value	0	0	0	0	0	0	0	0	
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r	r	r	r	r	r	r	r																																								
Flag	IOVP	X	X	IUVP	OFF	IIN_OCP	IIN_OCW	X																																								
Default Value	0	0	0	0	0	0	0	0																																								
7D	STATUS_TEMPERATURE	<p>Returns one byte of information with the status of the module's temperature related faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Flag</td> <td>OT_FAULT</td> <td>OT_WARN</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	OT_FAULT	OT_WARN	X	X	X	X	X	X	Default Value	0	0	0	0	0	0	0	0	
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r	r	r	r	r	r	r	r																																								
Flag	OT_FAULT	OT_WARN	X	X	X	X	X	X																																								
Default Value	0	0	0	0	0	0	0	0																																								
7E	STATUS_CML	<p>Returns one byte of information with the status of the module's communication related faults.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Flag</td> <td>COM</td> <td>DATA</td> <td>PEC</td> <td>Memory</td> <td>X</td> <td>X</td> <td>OTHER</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	COM	DATA	PEC	Memory	X	X	OTHER	X	Default Value	1	0	0	0	0	0	0	0	
Format	Unsigned Binary																																															
Bit Position	7	6	5	4	3	2	1	0																																								
Access	r	r	r	r	r	r	r	r																																								
Flag	COM	DATA	PEC	Memory	X	X	OTHER	X																																								
Default Value	1	0	0	0	0	0	0	0																																								

80	STATUS_MFR_SPECIFIC	<p>Returns one byte of information with other faults .</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Unsigned Binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Flag</td> <td>CAL APC</td> <td>OS P</td> <td>VDD UVLO</td> <td>SVI D</td> <td>VR_Hot</td> <td>eMTPB 00t</td> <td>eMTPU pload</td> <td>X</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Unsigned Binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Flag	CAL APC	OS P	VDD UVLO	SVI D	VR_Hot	eMTPB 00t	eMTPU pload	X	Default Value	0	1	0	1	0	0	0	0																																					
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Flag	CAL APC	OS P	VDD UVLO	SVI D	VR_Hot	eMTPB 00t	eMTPU pload	X																																																																												
Default Value	0	1	0	1	0	0	0	0																																																																												
88	READ_VIN	<p>Returns the value of the input voltage applied to the module.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	1	0	1	0	0	0	0	
Format	Literal Format. two's complement binary																																																																																			
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Function	Exponent				Mantissa																																																																															
Default Value	1	1	1	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	1	0	1	0	0	0	0																																																																												
89	READ_IIN	<p>Returns the value of the input current applied to the module.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Access</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> <td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	
Format	Literal Format. two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
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Default Value	1	1	1	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												

8B	READ_VOUT	<p>Returns the actual measured output voltage in the same format as set by the VOUT_MODE command (VID format).</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">VID format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">High Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">Low Byte</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	VID format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	High Byte								Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Low Byte								Default Value	0	0	0	0	0	0	0	0	
Format	VID format. two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	High Byte																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Low Byte																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												
8C	READ_IOUT	<p>Returns the value of the average total output current applied to the module.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	1	1	1	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	1	1	1	
Format	Literal Format. two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	1	1	1	1	1	1	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	1	1	1																																																																												
8D	READ_TEMPERAT URE_1	<p>Returns the temperature in °C (Literal Format) of the external sense element.</p> <table border="1"> <tr> <td>Format</td> <td colspan="8">Literal Format. two's complement binary</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="4">Exponent</td> <td colspan="4">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <td colspan="8">Mantissa</td> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	1	1	1	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	
Format	Literal Format. two's complement binary																																																																																			
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Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												

8E	READ_TEMPERAT URE_2	<p>Returns the temperature in °C (Literal Format) of the external sense element.</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Literal Format. two's complement binary</th> </tr> </thead> <tbody> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="4">Exponent</th> <th colspan="4">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="8">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td> </tr> </tbody> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	1	0	0	1	1	0	
Format	Literal Format. two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
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Function	Exponent				Mantissa																																																																															
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	1	0	0	1	1	0																																																																												
94	READ_DUTY_CYC LE	<p>Returns the duty cycle of controller in % (Literal Format).</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Literal Format. two's complement binary</th> </tr> </thead> <tbody> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="4">Exponent</th> <th colspan="4">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="8">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td> </tr> </tbody> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	1	1	1	0	1	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	1	1	0	1	0	0	0	YES
Format	Literal Format. two's complement binary																																																																																			
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Function	Mantissa																																																																																			
Default Value	0	1	1	0	1	0	0	0																																																																												
96	READ_POUT	<p>Returns the power being delivered to the load in W (Literal Format).</p> <table border="1"> <thead> <tr> <th>Format</th> <th colspan="8">Literal Format. two's complement binary</th> </tr> </thead> <tbody> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="4">Exponent</th> <th colspan="4">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> <tr> <td>Bit Position</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>Access</td> <td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td> </tr> <tr> <td>Function</td> <th colspan="8">Mantissa</th> </tr> <tr> <td>Default Value</td> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td> </tr> </tbody> </table>	Format	Literal Format. two's complement binary								Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Exponent				Mantissa				Default Value	0	0	0	0	0	0	0	0	Bit Position	7	6	5	4	3	2	1	0	Access	r	r	r	r	r	r	r	r	Function	Mantissa								Default Value	0	0	0	0	0	0	0	0	YES
Format	Literal Format. two's complement binary																																																																																			
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Exponent				Mantissa																																																																															
Default Value	0	0	0	0	0	0	0	0																																																																												
Bit Position	7	6	5	4	3	2	1	0																																																																												
Access	r	r	r	r	r	r	r	r																																																																												
Function	Mantissa																																																																																			
Default Value	0	0	0	0	0	0	0	0																																																																												

97	READ_PIN	Returns the power being delivered to the power stage in W (Literal Format).	YES								
		Format		Literal Format. two's complement binary							
		Bit Position		7	6	5	4	3	2	1	0
		Access		r	r	r	r	r	r	r	r
		Function		Exponent				Mantissa			
		Default Value		0	0	0	0	0	0	0	0
		Bit Position		7	6	5	4	3	2	1	0
		Access		r	r	r	r	r	r	r	r
		Function		Mantissa							
		Default Value		0	0	0	0	0	0	0	0
98	PMBUS_REVISION	Returns one byte indicating the module is compliant to PMBus Spec. 1.1 (read only)	YES								
		Format		Unsigned Binary							
		Bit Position		7	6	5	4	3	2	1	0
		Access		r	r	r	r	r	r	r	r
		Default Value		0	0	0	1	0	0	0	1
99	MFR_ID	Loads the unit with ASCII characters that contain the manufacturer's ID.	YES								
		Format		Unsigned Binary							
		Bit Position		7	6	5	4	3	2	1	0
		Access		r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
		Function		High Byte							
		Default Value		0	1	0	1	0	0	0	0
		Bit Position		7	6	5	4	3	2	1	0
		Access		r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
		Function		Low Byte							
		Default Value		0	1	0	1	1	0	0	0

D0	MFR_SPECIFIC_00	Returns module name information (read only).								
		Format	Unsigned Binary							
		Bit Position	7	6	5	4	3	2	1	0
		Access	r	r	r	r	r	r	r	r
		Function	High Byte							
		Default Value	0	0	0	0	0	0	0	0
		Bit Position	7	6	5	4	3	2	1	0
		Access	r	r	r	r	r	r	r	r
		Function	Low Byte							
		Default Value	0	0	0	0	0	0	0	1
D1	MFR_SPECIFIC_01	Provides access control for configuration register writes. Must be set to 0xB37C to enable register writes.								
		Format	Unsigned Binary							
		Bit Position	7	6	5	4	3	2	1	0
		Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
		Function	High Byte							
		Default Value	0	0	0	0	0	0	0	0
		Bit Position	7	6	5	4	3	2	1	0
		Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
		Function	Low Byte							
		Default Value	0	0	0	0	0	0	0	0
D2	MFR_SPECIFIC_02	Provides user to enable/disable SVID/PMBus command.								
		Format	Unsigned Binary							
		Bit Position	7	6	5	4	3	2	1	0
		Access	r	r	r	r	r	r	r/w	r/w
		Default Value	0	0	0	0	0	0	0	1
Note: Literal=11-bit mantissa (signed binary integer), 5-bit exponent (signed binary integer).										

DC-DC Converter Non-Isolated

Technical Specification DAM60N12D0V6GSGA

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 11. The preferred airflow direction for the module is in Figure 12.

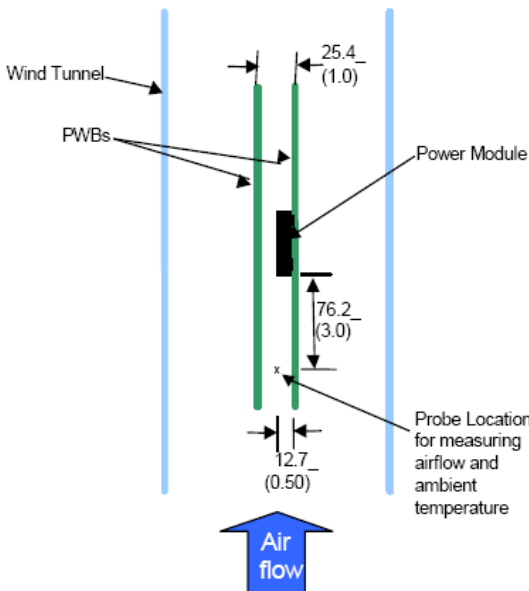


Figure 11. Thermal Test Setup.

The thermal reference points, T_{ref} used in the specifications are also shown in Figure 12. For reliable operation the temperatures at these points should not exceed OTP set value. The output power of the module should not exceed the rated power of the module ($V_{o,set} \times I_{o,max}$).

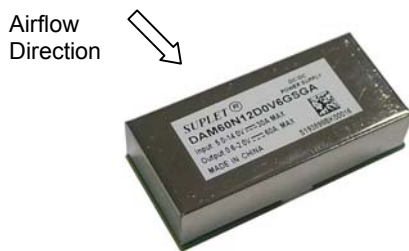


Figure 12. Recommended Airflow Direction

Soldering Information (Surface mounting Version)

Reflow Soldering Information

These power modules are large mass, low thermal resistance devices and typically heat up slower than other SMT components. It is recommended that the customer review data sheets in order to customize the solder reflow profile for each application board assembly.

The following instructions must be observed when SMT soldering these units. Failure to observe these instructions may result in the failure of or cause damage to the modules, and can adversely affect long-term reliability.

Typically, the eutectic solder melts at 217°C, wets the land, and subsequently wicks the device connection. Sufficient time must be allowed to fuse the plating on the connection to ensure a reliable solder joint. There are several types of SMT reflow technologies currently used in the industry. These surface mount power modules can be reliably soldered using natural forced convection, IR (radiant infrared), or a combination of convection/IR. For reliable soldering the solder reflow profile should be established by accurately measuring the modules pin connector temperatures.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L , +217 to +221°C for Sn/Ag/Cu solder alloys) for more than 30 seconds, and a peak temperature of +235°C on all solder joints is recommended to ensure a reliable solder joint. For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C. During reflow, T_P must not exceed +245°C at any time.

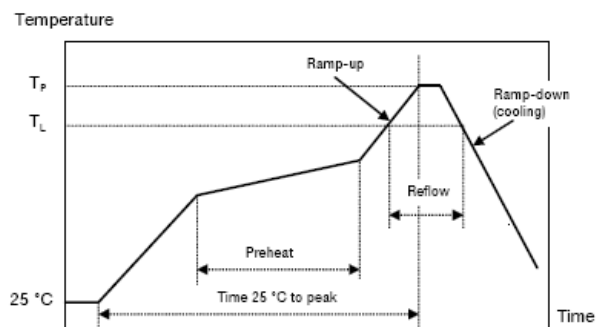


Figure 13. Recommended reflow profile.

DC-DC Converter Non-Isolated

Technical Specification DAM60N12D0V6GSGA

Reflow process specifications		Pb-free
Average ramp-up rate		3°C/s max
Solder melting temperature (lim)	T_L	+217°C
Time above T_L		30 s~90s
Minimum pin temperature	T_{pin}	+235°C
Peak product temperature	T_p	+245°C
Average ramp-down rate		6°C/s max
Time 25°C to peak		6 minutes max

Storage and Handling

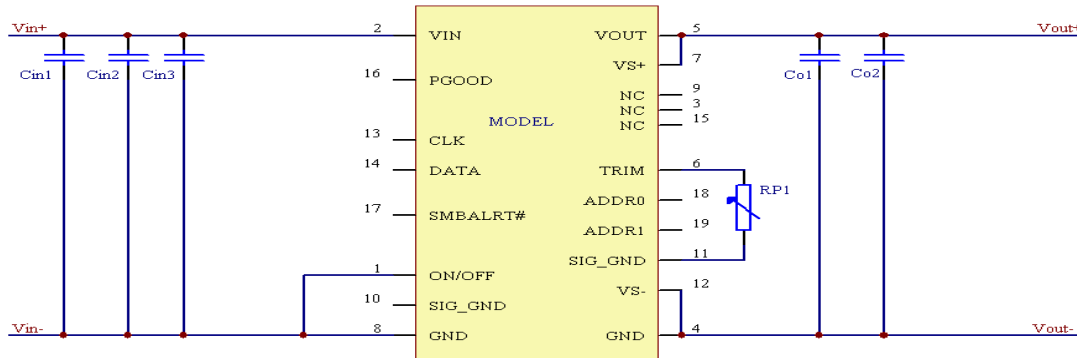
The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. B (Handling, Packing,

Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for max. MSL2 condition. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of $\leq 30^\circ\text{C}$ and 60% relative humidity varies according to the MSL rating (see J-STD-033B). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: $< 40^\circ\text{C}$, $< 90\%$ relative humidity.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly.

Application Circuit



Cin1 Decoupling cap - 1x0.01uF/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)

Cin2 4x47F/16V ceramic capacitor (e.g. EMK325BJ476MM-T(TAIYO)//GRM32ER61C476ME15L(MURATA)

Cin3 470uF/16V bulk electrolytic

CO1 Decoupling cap - 1x0.01 F/16V ceramic capacitor (e.g. Murata LLL185R71E103MA01)

CO2 4x47uF/6.3V ceramic capacitor (e.g. EMK325BJ476MM-T(TAIYO)//GRM32ER61C476ME15L(MURATA)

RTrim SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

Outline Diagram

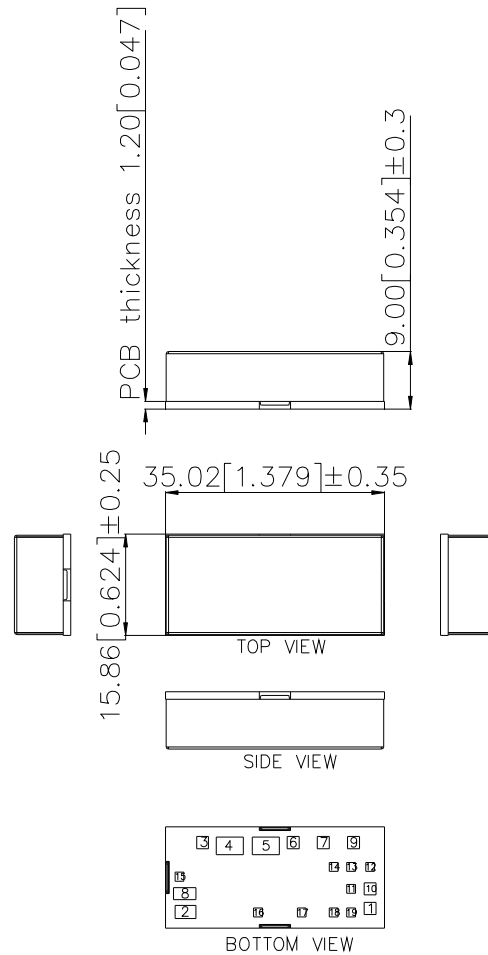


Figure14. Outline Diagram

Pin Designations

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	ON/OFF	Remote Control ON/OFF	11	SIG_GND	Signal GND
2	VIN	Input Voltage	12	VS-	Negative Sense
3	NC	No Connection	13	CLK	PMBus Clock
4	GND	Negative Output Voltage	14	DATA	PMBus Data

DC-DC Converter Non-Isolated

Technical Specification DAM60N12D0V6GSGA

5	VOUT	Output Voltage	15	NC	No Connection
6	TRIM	Output Voltage Adjustment	16	PG	Power Good
7	VS+	Positive Sense	17	SMBALERT#	PMBus Alarm
8	GND	Negative Output Voltage	18	ADDRESS0	PMBus Address Pinstrap 0
9	NC	No Connection	19	ADDRESS 1	PMBus Address Pinstrap 1
10	GND	Negative Output Voltage			

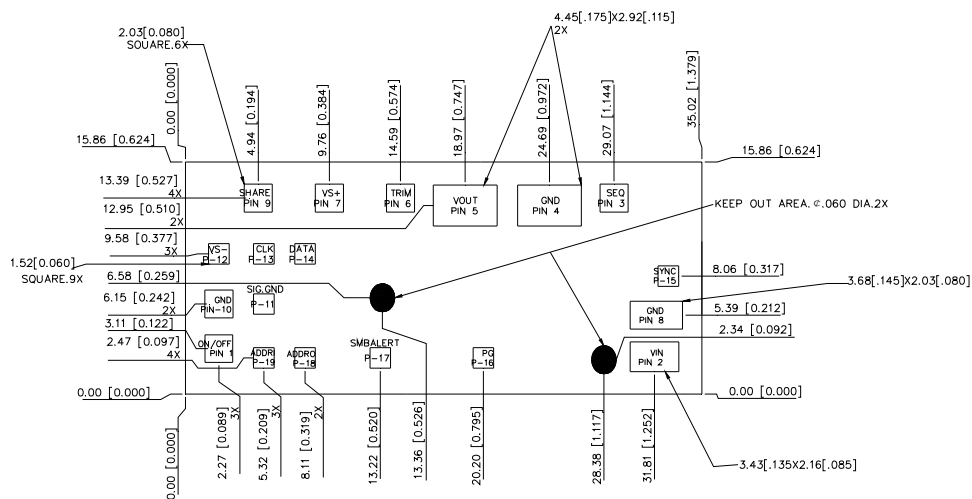


Figure15. Recommended Pad Layout

Note:

- Dimensions are in mm [inch].
Tolerances: $x.x \text{ mm} \pm 0.5 \text{ mm}$ [$x.xx \text{ in.} \pm 0.02 \text{ in.}$], $x.xx \text{ mm} \pm 0.25 \text{ mm}$ [$x.xxx \text{ in.} \pm 0.010 \text{ in.}$] (Unless otherwise indicated).
- PCB surface finish is Lead free HASL conducted by SN100C, and thickness is 2.54um~ 40um.

DC-DC Converter Non-Isolated

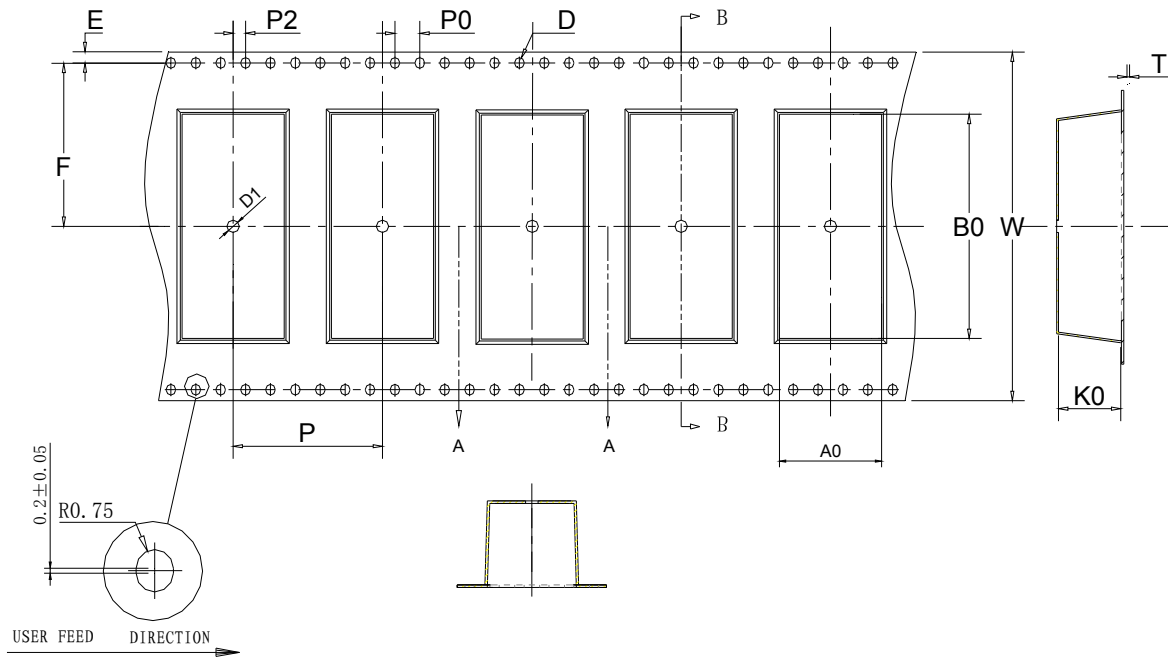
Technical Specification DAM60N12D0V6GSGA

Packaging Details

The modules are supplied in reel as standard.

All Dimensions are in millimeters.

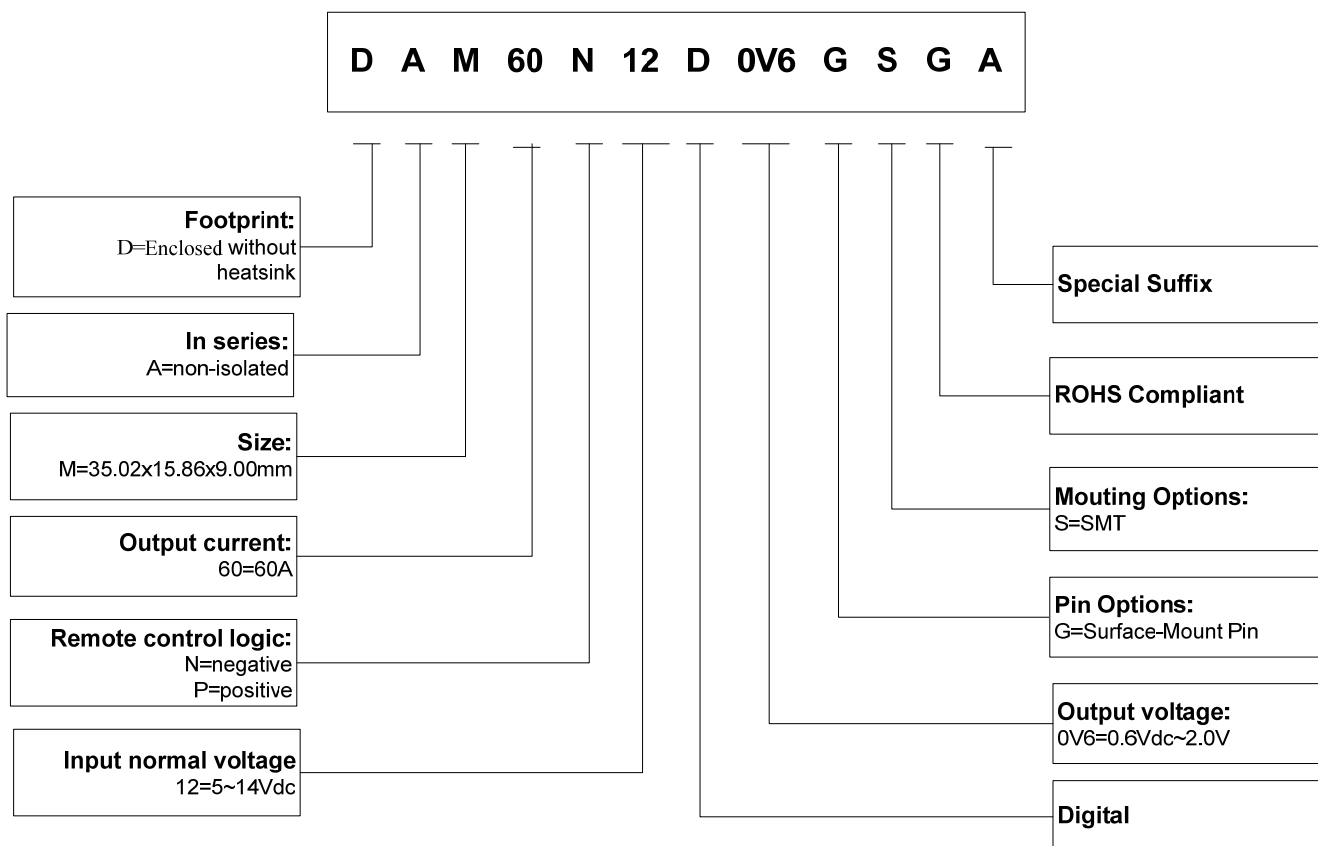
ITEM	W	A0	B0	K0	P	F	E	D	D1	P0	P2	t	13"	
DIM	56.0	16.4	36.0	10.5	24	26.20	1.75	1.50	2.00	4.00	2.00	0.5	Length/ tape	Capacity /tape
TOLE	+0.30 -0.30	+0.00 -0.10	+0.00 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.00	+0.10 -0.00	+0.10 -0.10	+0.15 -0.15	+0.05 -0.05	7.0m	250pcs



DC-DC Converter Non-Isolated

Technical Specification DAM60N12D0V6GSGA

Naming Rules On Models



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